What is claimed is:

1. A method of forming a sealing nitride layer overlaying a oxide layer in a contact opening of an integrated circuit, the method comprising:

forming a second layer of nitride overlaying a first layer of nitride to form the sealing nitride layer, the second layer of nitride further overlaying an exposed portion of a surface of a substrate in the contact opening and sidewalls of the contact opening; and

using reactive ion etching (RIE etch) without a mask to remove a portion of the second nitride layer adjacent the surface of the substrate in the contact opening to expose a portion of the surface of the substrate in the contact opening without removing portions of the second nitride layer covering the sidewalls of the contact opening.

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2. The method of claim 1, wherein the second layer of nitride is formed by low pressure chemical vapor deposition.

3. The method of claim 1, wherein the second layer of nitride is formed by plasma enhanced chemical vapor deposition.

4. The method of claim 1, wherein, at least a portion of the first layer of nitride remains overlaying the oxide layer after the RIE etch is applied.

5. The method of claim 1, wherein the RIE etch is applied for a pre-determined amount of time.

6. The method of claim 5, wherein the pre-determined amount of time is the time it takes to remove a portion of the second layer of nitride from the surface of the substrate in the contact opening.

7. A method of forming an integrated circuit, the method comprising:

forming a layer of oxide over a surface of a substrate;

forming a first layer of nitride overlaying the layer of oxide;

forming a contact opening through the first layer of nitride and the oxide layer to expose a portion of the surface of the substrate;

forming a second layer of nitride overlaying the first layer of nitride, the second layer of nitride also overlaying the exposed portion of the surface of the substrate in the contact opening and sidewalls of the contact opening; and

using a reactive ion etch (RIE etch) without a mask on the substrate for a pre-determined amount of time to remove a portion of the second layer of nitride overlaying the surface of the substrate in the contact opening without removing the portions of the second nitride layer overlaying the sidewalls of the contact opening, wherein the oxide layer is sealed by the first and second nitride layers.

8. The method of claim 7, wherein the contact opening through the first nitride layer and the oxide layer is done with a dry etch with one mask to form an anisotropic contact opening.

9. The method of claim 7, wherein the oxide layer is thermally grown.

10. The method of claim 7, wherein the oxide layer is deposited.

11. The method of claim 7, wherein the first and second layers of nitride are formed by low pressure chemical vapor deposition.

12. The method of claim 7, wherein the first and second layers of the nitride are formed by plasma enhanced chemical vapor deposition.

13. The method of claim 7, wherein, at least a portion of the first layer of nitride remains overlaying the oxide layer after the RIE etch is applied.

14. A method of forming semiconductor devices in an integrated circuit comprising:

forming a plurality of device regions of a first conductivity type in a substrate adjacent a surface of the substrate;

forming an oxide layer over a surface of a substrate;

patterning the oxide layer to expose pre-selected portions of the surface of the substrate;

forming a first layer of nitride overlaying the oxide layer and the exposed portions of the surface of the substrate;

implanting ions of a second conductivity type through the layer of nitride into the substrate to form device regions of the second conductivity type, wherein remaining portions of the oxide layer under the nitride layer selectively stop the ions from entering the substrate to selectively define edges of the device regions of the second conductivity type;

forming contact openings to expose a portion of each of the device regions of the first and second conductivity type in the substrate;

forming a second layer of nitride over the first layer of nitride, the second layer of nitride also overlaying the exposed portions of each of the device regions in their associated contact openings and sidewalls of each of the contact openings; and

exposing the substrate to a reactive ion etch (RIE etch) for a pre-determined amount of time to remove portions of the second layer of nitride adjacent a surface of each device region in an associated contact opening, wherein the substrate is not exposed to the RIE etch long enough to remove all of the portions of the second nitride layer overlaying the respective sidewalls of each of the contact openings so that the oxide layer remains sealed by the first and second layers of nitride.

15. The method of claim 14, wherein the contact openings made through the first nitride layer and the oxide layer to associated device regions are done with a dry etch with a single mask to form anisotropic contact openings.

16. The method of claim 14, wherein the first and second layers of nitride are formed by low pressure chemical vapor deposition.

17. The method of claim 14, wherein the first and second layers of the nitride are formed by plasma enhanced chemical vapor deposition.

18. The method of claim 14, wherein, at least a portion of the first layer of nitride remains overlaying the portions of oxide layer after the RIE etch is applied.

19. An integrated circuit comprising:

a substrate;

a plurality semiconductor devices formed in the substrate, some of the semiconductor devices having device regions formed adjacent a surface of the substrate;

a layer of oxide overlaying the surface of the substrate;

a first layer of nitride overlaying the layer of oxide, the first layer of nitride and the layer of oxide having a plurality of contact openings extending to select device regions in the substrate; and

portions of a second layer of nitride overlaying sidewalls of each contact opening, wherein the portions of the second layer of nitride overlaying the oxide layer in the sidewalls are thinner than the first layer of nitride overlaying the rest of the layer of oxide.

20. The integrated circuit of claim 19, wherein at least one of the semiconductor devices is a bipolar transistor.

21. The integrated circuit of claim 20, wherein the at least one bipolar transistor comprises:

a base region formed in the substrate adjacent the surface of the substrate, the first and second layers of nitride and the oxide layer having a contact opening to the base region;

an emitter formed in the base region, the second layer of nitride having a contact opening to the emitter; and

a collector contact formed in the substrate an predefined distance from the base region, the second layer of nitride having a contact opening to the collector contact.

22. The integrated circuit of claim 21, wherein the at least one bipolar transistor further comprises:

a metal base contact region formed in the contact opening to the base region;

a metal emitter contact region formed in the contact opening to the emitter; and

a metal collector contact region formed in the contact opening to the collector contact.